

# Improving wafer map classification in Industry 4.0

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**Abstract**—At the heart of Industry 4.0, lies the automation of manufacturing processes and interoperability of corresponding applications, in most cases utilizing Cyber-Physical Systems and Internet of Things. Used within diverse industrial areas across the world, these concepts gained more importance in recent years. In the semiconductor industry, continuous improvement of all involved processes is achieved by utilizing these concepts in many different stages of the manufacturing process. This work proposes a machine learning framework that on one hand enhances wafer map classification in the testing stage of semiconductor devices, and on the other hand fulfills the requirements and demands of all involved stakeholders in adopted engineering processes. The core of the proposed system is the Wafer Health Factor, a machine learning framework that detects process deviations in analog wafer test data through pattern recognition. Additional integration of Radon-based features, as well as the use of an ensemble classification framework, boosts model performances in the presented real-world application scenario significantly. Moreover, we also show that the proposed framework performs well on two benchmark data sets from literature, even on small training data sets. We conclude, that the presented framework improves the performance of pattern recognition tasks in real-world applications and thus, enables the automatic and early detection of deviations within semiconductor manufacturing processes.

**Index Terms**—Arrowhead Tools, analog wafer test data, engineering process, ensemble classification, machine learning, pattern recognition, Radon transform

## I. INTRODUCTION

The fourth Industrial Revolution brought major changes in many industrial areas, heavily improving existing applications. One of the most important concepts within semiconductor manufacturing is the automation of Internet of Things (IoT) related processes, which is heavily influenced by robotics [1] and machine learning (ML) algorithms to enable adopted systems to be smarter and perform more efficient. Due to the nature of related tasks, a high level of efficiency and accuracy must be achieved when implementing automation tools, ultimately preventing errors and mistakes which otherwise can cause serious economic damage [2].

The main areas of research that have gained increased attention in recent years are reliability [3], performance [4] and cyber security [5]. Systems using IoT frameworks produce a lot of data [6] due to the presence of many sensors and

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actuators, for instance, enabling predictive maintenance with minor manual interaction [7]. Moreover, they are also gaining importance in current digitalization projects such as the Arrowhead Tools project [8], the biggest European digitalization project today which deals with these systems merging with modern technologies such as IoT, cloud computing systems, machine learning and artificial intelligence, to make legacy systems more efficient.

Most of the existing research regarding ML within semiconductor manufacturing focuses on the development of algorithms for tasks such as predictive maintenance of equipment [9] as well as pattern recognition for wafers [10].

It is evident, that IoT plays a big role in semiconductor manufacturing nowadays. Schneider et al. [2] deployed a system in the 200mm Infineon Dresden Wafer Fabrication Plant which is ramping up wafer production and transportation enabling higher throughput, significantly lowering engineering costs, and reducing the workload on operators.

Some more recent research has focused on and demonstrated how state-of-the-art ML techniques can be incorporated into manufacturing processes, such as predictive model-based quality inspection of surface-mount components at a Siemens electronics plant [11]. Ramezankhani et al. [12] also proposed an active transfer learning framework that was applied to a case study that considers an aerospace composite manufacturing plant.

Due to the complexity involved in the semiconductor manufacturing process, pattern recognition is very challenging because some observed patterns tend to occur more often than others. Thus, in real-world applications and implementations, the lack of sufficient fully-descriptive wafer test data for less occurring patterns restricts the performance of predictive ML models [10].

## II. THE ENGINEERING PROCESS MODEL FOR ML APPLICATIONS IN THE SEMICONDUCTOR INDUSTRY

In this work, we aim to introduce a complete framework to demonstrate how ML algorithms can be used to perform pattern recognition on analog wafer test data embedded in a series of engineering processes involving various stakeholders. The framework is tailored to an actual use case coming from the semiconductor industry. Figure 1 depicts the developed multi-stakeholder automation process including each involved stakeholder (StkH). To reflect relevant needs regarding system maintenance, user training, and the evolution of the system,

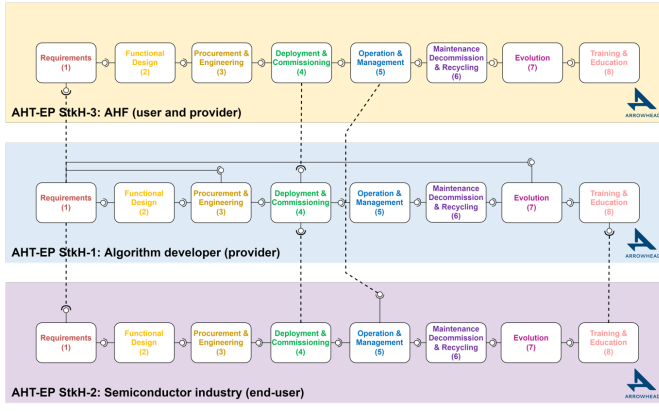


Fig. 1: Multi-stakeholder automation process of the investigated semiconductor use case. The AHT-EP is utilized to model the engineering process of each stakeholder individually and capture interactions between them.

the Arrowhead Tools Engineering Process (AHT-EP) is used. The AHT-EP is an extension of the automation engineering standard *IEC 81346*, enriched with the three engineering steps called Maintenance Decommissioning & Recycling, Evolution and Training & Education. A general and detailed description of the AHT-EP is given by Urgese et al. [13]. In Figure 1, StkH-1 is the algorithm developer and encompasses activities like collecting requirements (1), creating a concept / choosing an approach (2), implementing the algorithm (3), making the algorithm applicable (4), usage of the application (5), maintaining the application (6), further developing/improving the functionality (7) and providing user manuals / supporting users (8). StkH-2, the semiconductor industry, is the end-user of StkH-1. Therefore, an interface to use the developed algorithms needs to be provided (4). At StkH-2, this then also needs an adjustment of existing requirements (1) and related training activities (8) for the end-users. StkH-3 is the Arrowhead Framework (AHF), the software component that addresses the IoT-based automation by abstracting all involved IoTs to services. A thorough introduction to the AHF is given by J. Delsing [14].

### III. ENHANCED MACHINE LEARNING PIPELINE FOR PATTERN RECOGNITION

It is imperative to develop a classification framework that can produce robust models within low-data regimes which enable accurate predictions. Schrunner et al. [10] introduced the Wafer Health Factor (WHF), which enables the assessment of wafer maps by combining domain knowledge with pattern recognition. They already introduced the usage of Rotational Local Binary Patterns (RLBP) and Histogram of oriented Gradients (HoG) features in their work which proved to extract sufficient information from the wafer maps to reliably predict process patterns on them. The proposed scheme enhances the initially proposed framework by Schrunner et al. [10] by introducing Radon-transform-based features in combination with ensemble classification. The scheme depicted in Figure

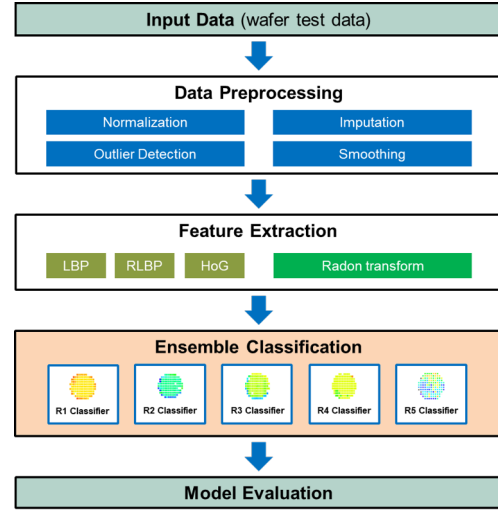


Fig. 2: Proposed ML framework for pattern recognition within analog wafer test data.

2 is proposed, which enables wafer map classification by utilizing one-vs-rest (OVR) ensemble classification. It combines extracted features from the input data (a detailed description is given in section IV) using Radon transforms, RLBP, and HoG as input for the ML model. The proposed scheme can be applied in diverse scenarios due to its flexibility in data preprocessing: Using different techniques for normalization, imputation, outlier detection, and smoothing, the scheme can be adjusted for different properties of emerging pattern types.

The proposed framework resolves the aforementioned challenges, especially achieving good results in low-data regimes for analog wafer test data.

#### A. The Radon transform

The Radon transform projects a function  $f$  on the plane to the two-dimensional space of lines in the plane by utilizing the line integral of  $f$  over this line. This concept can also be applied to images, where the values of the function  $f$  are simply the pixels of the image. The Radon transform  $R(\rho, \theta)$  of an  $m \times n$  image  $f$  can be approximated with the formula

$$R(\rho, \theta) = \sum_{i=1}^m \sum_{j=1}^n f(i, j) \cdot \delta(i \cos \theta + j \sin \theta - \rho) \quad (1)$$

where  $f(i, j)$  is the pixel in row  $i$  and column  $j$  of image  $f$ ,  $\delta$  is a Dirac-Delta function and  $\rho$  and  $\theta$  are parameters which represent the distance from the origin to the resulting projection and the angle from the x-axis, respectively [15]. This formula in combination with a sufficiently fine discretization of the parameter space yields an approximation to the Radon transform of the image. Figure 3 depicts the idea of how to use the Radon transform on wafer maps: the output of the Radon feature calculation are six sets of features obtained from applying different statistical measures to the Radon transform of the wafer map.

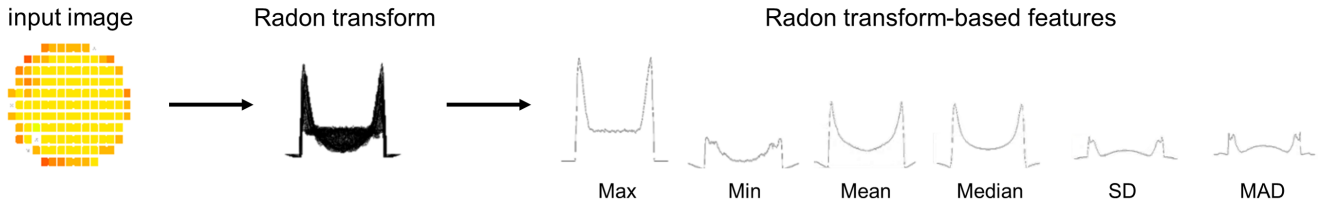


Fig. 3: Generation of Radon transform-based features from a wafer map. Instead of using the Radon transform directly, 6 statistical measures are calculated for each x-value: maximum value (Max), minimum value (Min), the average (Mean), the median (Median), the standard deviation (SD) and the median absolute deviance (MAD).

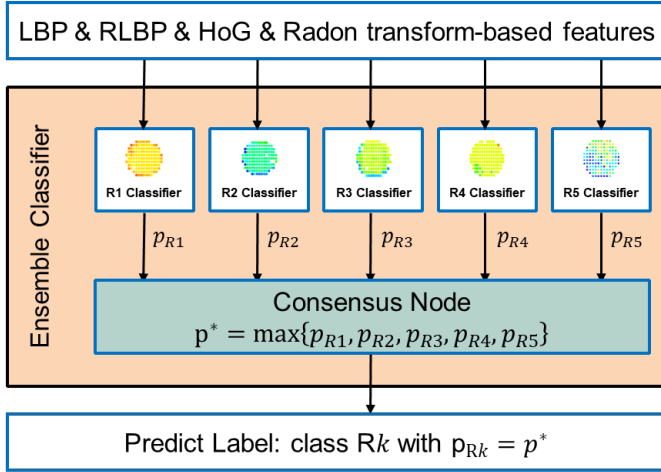


Fig. 4: Structure of the implemented ensemble classifier for *dataset\_1*. The features extracted via the LBP, RLBP, HoG and Radon transform-based feature descriptors are the input for each binary classifier. The negative class for each classifier comprises all other patterns, e.g. for the R1 classifier the negative class consists of a stratified set over classes R2 to R5.

### B. Ensemble Classification

In general, ensemble classification models combine predictions obtained from a set of different - not necessarily binary - classifiers that are trained on the individual respective patterns that are present in the data set. The structure of the proposed ensemble classifier is depicted in Figure 4. Each model can be viewed as an expert for a particular pattern type. The outputs of the individual classifiers are obtained as probability values which are then passed onto a consensus node inside the ensemble classifier. The main job of the consensus node is the comparison of the different predicted probabilities from the individual classifiers and provides a final classification result. Thus, the predicted label is obtained by performing a soft classification on the predicted probabilities by finding the maximum probability and predicting the respective class label. This implies that each binary model provides a probability value for the wafer map passed through the pipeline and the model with the highest probability is seen to be the one providing the best suitable classification for that wafer map.

The proposed framework utilizes an OVR ensemble classifier for each of the analyzed data sets. To be precise, the ensemble consists of binary random forest classifiers, one for each occurring pattern type.

## IV. SEMICONDUCTOR USE CASE STUDY

In most semiconductor manufacturing applications, pattern recognition is performed on so-called pass/fail maps. In these pass/fail maps, a device is marked either 0 or 1 depending on whether it is tested as pass or fail. Recent research has shown that most pattern recognition algorithms yield fairly accurate classification and prediction results on pass/fail maps.

Within this paper, we strive to react earlier, hence, utilizing the analog wafer maps themselves as input for the pattern recognition pipeline. In general, the input data consist of 3 components: metadata (logistic information such as lot and wafer number, device coordinates, various timestamps, etc.), test parameter values (mainly corresponding to analog tests), and test results (pass/fail information, type of error, etc.) [16].

The proposed ML framework can provide useful information about the manufacturing process, enabling a faster reaction to occurring problems. Furthermore, compared to conventional deep learning approaches, our models can be reliably trained with significant small training sets. In the following sections, we show the applicability of the proposed ML framework on synthetic as well as real-world semiconductor data sets.






### A. Experimental Setup

The proposed ML framework is assessed on different data sets, including real-world productive analog wafer test data as well as synthetic data. The following enumeration lists all evaluated data sets with a brief description.

- *dataset\_1*: analog wafer test data comprising 375 wafer maps (all from one electrical test), each showing one of 5 distinct pattern types.
- *dataset\_2*: benchmark data set *MixedWM38* with more than 38000 pass/fail maps and 9 distinct pattern types, introduced by Wang et. al [17].
- *dataset\_3*: synthetic wafer test data, containing 5000 simulated analog wafer maps over 5 different pattern types, available at ZENODO [18].

Initial experiments showed, that 10 wafer maps per pattern class are sufficient to train a decent model. Therefore, the

TABLE I: Detailed information on the five pattern types (R1-R5) for *dataset\_1*.

Name	#maps	Example	Description
R1	58		circular pattern on the border
R2	87		crescent on one side of the border
R3	82		two crescents on opposite sides
R4	89		spot where size and position can differ
R5	59		any other pattern besides R1-R4

training set for *dataset\_1* consists of 10 sampled wafer maps for each pattern type (50 in total), detailed information on the pattern types is provided in Table I. For each of *dataset\_2* and *dataset\_3*, 100 wafer maps are sampled per pattern class to guarantee a balanced training set. The test sets for each scenario consist of all wafer maps which are not used within the training phase. Additionally, cross-validation is used to lower the impact of chosen wafer maps in the training set on the prediction performance.

For each of the aforementioned data sets, prior analyses were conducted to identify the optimal choice and combination of preprocessing techniques. The techniques used in these analyses include standard and robust scores for normalization (i.e. mean/standard deviation and median/interquartile ranges), neighborhood-based interpolation for imputation, part average testing [19] for outlier detection and the use of Markov Random Fields [20] for smoothing the data.

The evaluation procedure for the proposed ML framework encompasses the following key aspects:

- different feature sets: To show the impact of the Radon features on the classification result, four different feature sets are compared to each other as described in Table II.
- two distinct modeling approaches: the proposed ensemble approach is compared to a single model approach.
- cross-validation: to lower the influence of single wafer maps on the classification result, stratified repeated random sub-sampling validation is implemented.
- varying training-to-test ratio: to show the efficiency of the proposed ML framework on pass/fail or synthetic wafer test data, different training dataset sizes are used, ranging from 1% to 90% of the total amount of available wafer maps.

#### B. Comparison of the two modeling approaches

The performance of both modeling approaches is compared for the real-world data set *dataset\_1*. As can be seen in Table III, the ensemble approach outperforms the single model approach in all considered cases. Moreover, *Set 4*, which contains the Radon features, performs the best with a single exception.

TABLE II: Investigated feature sets, combining different feature descriptors, to analyze the impact of the added Radon features on the prediction.

Name	(R)LBP	HoG	Radon(max)	Radon(all)	# features
<i>Set 1</i>	×	×			146
<i>Set 2</i>				×	858
<i>Set 3</i>			×		143
<i>Set 4</i>	×	×	×		289

#### C. Impact of the training-to-test ratio on prediction

For analog wafer test data, labels are not provided standard-wise but need to be assigned manually specifically for classification. Therefore, the impact of the training-to-test ratio on the performance is investigated for *dataset\_2* and *dataset\_3*. Figure 5 shows that by using more than 10 wafer maps per class, differences between both approaches cannot be observed. Thus, the following analysis focuses only on the ensemble model approach. For *dataset\_2*, as shown in Table IV, *Set 4* performs best in the 10 wafer maps scenario. Although the average F1 score is slightly higher for *Set 2*, the significantly lower number of corresponding features for *Set 4* is a strong argument for using this feature set.

In contrast, the 80 wafer maps scenario shows a different picture. Leaving aside the vacuous results for *dataset\_3*, *Set 1* is performing better on average than *Set 4* which hints that additional Radon features are not needed for *dataset\_2*. A possible cause may be in the data itself. Compared to *dataset\_1* and *dataset\_3*, *dataset\_2* consists of pass/fail wafer maps, which have to be transformed on a continuous 0-1 scale to fit in the proposed ML framework.

## V. CONCLUSION

The presented work validates the use of Radon-based features in conjunction with ensemble classification for pattern recognition tasks in semiconductor applications. Key contributions of this work can be summarized as follows:

- 1) Introduction of an ML framework for pattern type classification which is embedded in an AHT-EP to improve engineering process design of a use case within the semiconductor industry.
- 2) Usage of a combination of (R)LBP & HoG features and Radon-based features as input for the pattern recognition algorithm to improve the classification performance, where the conducted experiments suggest, that using Radon-based features alone is not sufficient.
- 3) Introduction of an ensemble-based modeling approach that outperforms the single model approach for analog wafer test data, whereas similar results are observed for sufficiently large training-to-test ratios when dealing with pass/fail or synthetic wafer test data.

Taking the above aspects into account, future work will be laid on the scalability of the proposed ML framework to other real-world semiconductor products and the identification of necessary modifications to the framework to enable the use of deep learning architectures.

TABLE III: Pattern type classification results for *dataset\_1*. Provided are the F1 scores for each pattern class (R1-R5) for both approaches (single model and ensemble) and feature sets (Set1-Set4). The best performing feature set for each pattern is printed bold.

Data Set	Pattern	Set 1	Set 2	Set 3	Set 4
<i>dataset_1</i>	R1	67.79	66.05	64.15	<b>75.63</b>
	R2	<b>77.02</b>	70.19	61.07	71.05
	R3	<b>62.68</b>	50.35	49.61	61.31
	R4	<b>75.25</b>	60.24	62.26	73.21
	R5	<b>81.87</b>	48.80	40.84	66.15
Average		<b>73.58</b>	59.77	56.07	70.95

(a) Single model approach.

Data Set	Pattern	Set 1	Set 2	Set 3	Set 4
<i>dataset_1</i>	R1	78.50	76.49	74.56	<b>81.77</b>
	R2	82.34	80.05	76.54	<b>83.50</b>
	R3	<b>72.09</b>	67.25	61.78	70.64
	R4	78.51	71.70	68.45	<b>82.89</b>
	R5	84.45	79.69	78.22	<b>85.88</b>
Average		79.18	75.04	71.91	<b>82.04</b>

(b) Ensemble approach.

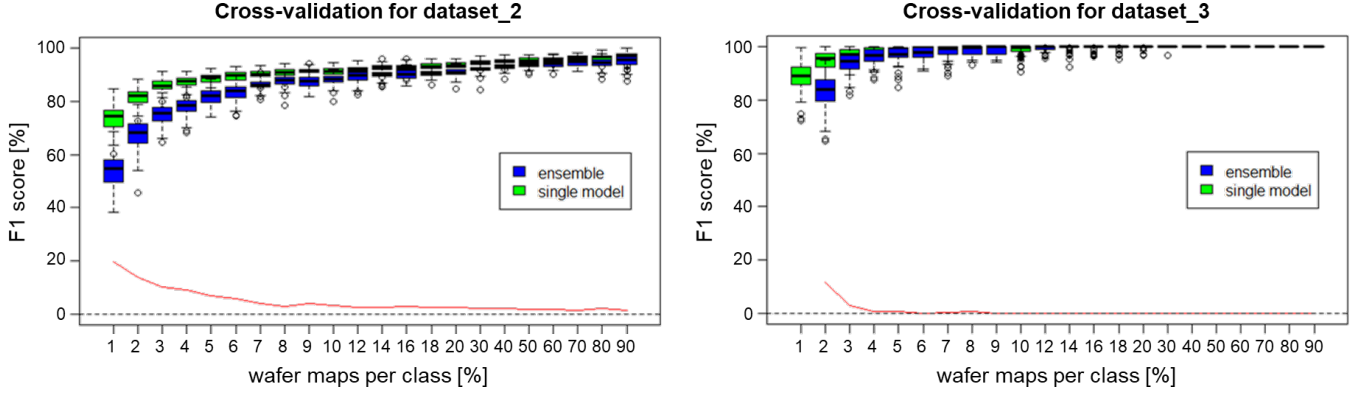


Fig. 5: Comparison of both modelling approaches (single model and ensemble) for varying training-to-test ratio on *dataset\_2* and *dataset\_3*. Depicted are the boxplots of the total F1 scores obtained from applying random sub-sampling cross-validation for 100 runs. The red line shows the difference of medians from both approaches.

TABLE IV: Pattern type classification results for *dataset\_2* and *dataset\_3*. Provided are the F1 scores for each pattern class (C1-C9 and Z1-Z5, respectively) for different training dataset sizes (80 and 10, respectively) and feature sets (Set1-Set4) for the ensemble approach. The best performing feature set for each pattern is printed bold.

Data Set	Pattern	Set 1	Set 2	Set 3	Set 4
<i>dataset_2</i>	C1	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>
	C2	<b>95.09</b>	86.44	83.86	92.43
	C3	<b>97.32</b>	87.88	83.63	93.08
	C4	88.80	<b>93.13</b>	84.79	85.99
	C5	93.82	<b>96.69</b>	88.87	91.02
	C6	<b>96.96</b>	96.66	94.48	96.28
	C7	97.25	<b>98.28</b>	97.89	97.94
	C8	93.38	94.68	<b>95.85</b>	95.38
	C9	97.14	98.10	97.85	<b>97.90</b>
Average		<b>95.53</b>	94.65	91.91	94.45
<i>dataset_3</i>	Z1	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>
	Z2	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>
	Z3	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>
	Z4	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>
	Z5	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>
Average		<b>100.00</b>	<b>100.00</b>	<b>100.00</b>	<b>100.00</b>

(a) Training on 80 wafer maps per pattern class.

Data Set	Pattern	Set 1	Set 2	Set 3	Set 4
<i>dataset_2</i>	C1	99.59	99.28	99.48	<b>99.91</b>
	C2	80.45	78.28	75.20	<b>80.63</b>
	C3	<b>88.45</b>	83.27	74.08	84.84
	C4	64.66	<b>77.14</b>	71.05	69.98
	C5	88.91	<b>89.39</b>	80.50	81.69
	C6	83.50	88.18	81.67	<b>89.21</b>
	C7	94.58	92.97	<b>96.97</b>	96.39
	C8	82.40	86.73	<b>88.75</b>	88.04
	C9	94.70	91.58	94.81	<b>95.92</b>
Average		86.36	<b>87.42</b>	84.72	87.40
<i>dataset_3</i>	Z1	98.24	95.16	98.60	<b>99.89</b>
	Z2	<b>99.69</b>	99.46	90.85	99.42
	Z3	97.19	<b>99.89</b>	98.12	98.75
	Z4	<b>98.90</b>	93.99	96.67	98.45
	Z5	97.74	<b>99.50</b>	93.63	99.42
Average		98.35	97.60	95.57	<b>99.19</b>

(b) Training on 10 wafer maps per pattern class.

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